Report Documentation Page

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The original document contains color images.

14. ABSTRACT
This month in Task 1.1 we made changes to two masks (Metal 3 and Dielectric) to improve the performance of the circuit breaker. Both double-side-polished (DSP) and silicon-on-insulator (SOI) wafers were processed using the revised masks.

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Monthly Status Report • November 2010
Covering the Period 1 November through 30 November 2010

POWER MEMS DEVELOPMENT

Contract N00014-09-C-0252
Submitted in accordance with Deliverable A001 - Monthly Technical and Financial
SRI Project P19063

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MEMS RESETTABLE CIRCUIT BREAKER (TASK 1.1) AND MEMS SWITCH FOR DC-DC VOLTAGE CONVERTERS (TASK 1.2)

Task 1.1 Contributors: Sunny Kedia, Weidong Wang, Susana Stillwell

Task 1.1 Deliverable: 10 prototype packed MEMS-based resettable circuit breakers for testing and analysis in ONR laboratories.

Task 1.2 Contributors: Sunny Kedia, Shinzo Onishi, Scott Samson, Drew Hanser

Task 1.2 Deliverable: Functional MEMS-based DC-DC converter in a vacuum package.

Summary: This month in Task 1.1 we made changes to two masks (Metal 3 and Dielectric) to improve the performance of the circuit breaker. Both double-side-polished (DSP) and silicon-on-insulator (SOI) wafers were processed using the revised masks.

In Task 1.2 we had previously identified that the long buffered oxide etch (BOE) causes the Metal 1 (Cr-Au) to float away during the BOE release step. In processing the wafers for the voltage converter, an ashing step is performed prior to the Metal 1 deposition to remove any undeveloped resist. This step results in the formation of a native oxide on exposed silicon, which is then etched during the BOE process. This undercuts the deposited metal and results in the metals floating away. To improve the adhesion of the metal to the structure silicon, we developed a BOE etch and pre-sputter experiment for the wafers prior to the Metal 1 deposition. SOI wafers with these short BOE and pre-sputter steps were fabricated. The fabricated wafers were then diced, and the chips are currently being released and tested.

We also continued development of the second cantilever fabrication technique using ProLIFT, a sacrificial polymer resist. We performed short-loop experiments to optimize the release of SiO_2 cantilevers using the ProLIFT. Using the data from the short-loop experiments, we developed a full wafer fabrication method and processed two wafers. We diced chips from these wafers for release and testing.

DIAMOND HEAT SPREADER OR HEAT SINK FOR HIGH-POWER MEMS SWITCH APPLICATIONS (TASK 1.3)

Contributors: Priscila Spagnol, Shinzo Onishi, Drew Hanser, Weidong Wang, Sunny Kedia, John Bumgarner

Deliverable: Prototype device fabricated on a thin-film diamond heat spreader layer and individual samples of diamond on Si or other suitable substrates for material evaluation.

Summary: No work was done this month on Task 1.3.

POSITRON TRAPPING AND STORAGE (TASK 2)

Contributors: Ashish Chaudhary, Friso van Amerom, Tim Short

Deliverable: A minimum of four MEMS-based trap structures for RF trapping of electrons

Summary: In Task 2 we modified the electron trap test setup to reduce the voltage spill-over from the high-voltage components and RF pickup from the trap. We designed new aluminum flanges for capturing the electrons and will test these components next month.

FINANCIAL STATUS

R&D Status Report

Program Financial Status

15 July 2009 through 27 November 2010

Contract Item No.	Current Funding	Current Period Expenses	Cumulative Expenses	% Budget Complete
0001	$1,829,849	$68,447	$1,541,051	84%
Project Commitments		1,122	213,934	
Total	$1,829,849	$69,569	$1,754,985	

Based on currently authorized work:

Is current funding sufficient for the current fiscal year (FY)? (Explain if NO) **Yes**

What is the next FY funding requirement at current anticipated levels **N/A** (**base fully funded)**